# LAYERED LDPC DECODING ARCHITECTURES: BRIDGING THE GAP FROM ALGORITHMS TO IMPLEMENTATIONS

Author: Oana AMARICĂI-BONCALO

## Abstract

This thesis presents the research and academic achievements during the 2014-2019 period. Moderncommunication and storage standards require efficient Forward Error Correction (FEC). Due to their excellent error correction capability, Quasy-Cyclic Low-Density Parity-check codes (QC-LDPC) are a class of codes employed in wireless standards, digital video broadcasting, and non-volatile semiconductor memories.

This fact prompted the research direction we have pursued during the last 5 years, mainly the study of QC-LDPC decoder architecture trade-offs and optimizations. More specifically, within the framework of the project DIAMOND - Message Passing Iterative Decoders based on Imprecise Arithmetic for Multi-Objective Power-Area Delay Optimization -, in collaboration with researchers from CEA-LETI Grenoble (dr. Valentin Savin), and ENSEA Cergy-Pontoise (prof. David Declercq),we have tried to exploit the advantages of implementing imprecise operations in Low-Density Parity-Check (LDPC) decoder architectures, in order to optimize the cost/area/power consumption. The original project goals – to develop hardware architectures that use imprecise arithmetic – have been largely expanded due to the very favorable research results. The contributions presented in this thesis closely follow the DIAMOND project.

A key contribution of this related to the data hazards due to the late update effect caused by memory access time and pipeline. Furthermore, if implementation-wise, the message memory uses banks made of Static Random Access Memory (SRAM) blocks, the access patterns according to the code graph also introduce data conflicts.

We approached this problem from two directions (1) A set of offline algorithms has been proposed such that an almost optimum message memory mapping and access scheduling that avoid RAW hazards is generated. (2) Architecture aware code design for application where the LDPC code is not fixed. The proposed algorithm builds on

a well known construction algorithm - Progressive Edge Growth (PEG).The proposed architecture aware PEG (AL-PEG) extends the original PEG by adding new constraints related to pipeline and message memory mapping.

The full thesis at:
http://www.upt.ro/Informatii_teze-de-abilitare-sustinute_285_ro.html

## Habilitation Commission

**Prof. dr. ing. Adina Magda Florea**
University Politehnica Bucharest
**Prof. dr. ing. Sergiu Nedevschi**
Technical University of Cluj-Napoca
**Prof. dr. ing. Mircea Popa**
Politehnica University Timișoara